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Damage mechanics of microelectronics solder joints under high current densities

Hua Ye, Cemal Basaran ^{*}, Douglas C. Hopkins

*UB Electronic Packaging Laboratory, State University of New York at Buffalo, SUNY,
101 Ketter Hall North Campus, Buffalo, NY 14260-4300, USA*

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Abstract

The electromigration damage in flip chip solder joints of eutectic SnPb was studied under current stressing at room temperature with a current density of $1.3 \times 10^4 \text{ A/cm}^2$. The height of the solder joints was 100 μm . The mass accumulation near anode side and void nucleation near cathode were observed during current stressing. The nano-indentation test was performed on solder joints for electromigration test. Surface marker movement was used to measure the atomic flux driven by electromigration and to calculate the product of effective charge number and diffusivity, $D \times Z^*$, of the solder at room temperature. The effective charge number can be extracted with the solder diffusivity at room temperature known. Pb phase coarsening was observed during current stressing.

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1. Introduction

The trend in flip chip and ball grid array packaging to increase I/O count drives the interconnecting solder joints to be smaller in size and, thus, have higher current density. The current densities will increase further as chip voltage decreases and absolute current level increases. The same trend in current densities in interconnecting solder joints is also occurring in flip chip power semiconductors and evolving system-on-package power processors (Paulasto-Krockel and Hauck, 2001; Liu et al., 2000a). A physical limit to increasing current density in both microelectronics and power electronics is electromigration. Electromigration of interconnect metal lines is the major failure phenomenon in ICs, but a seldom recognized reliability concern for solder joints. Most of the published literature on electromigration focused on thin pure metal lines, and little on present day solder interconnects (Brandenburg and Yeh, 1998; Lee et al., 2001; Lee and Tu, 2001; Liu et al., 1999, 2000a,b).

^{*}Corresponding author. Tel.: +1-716-645-2114/2429; fax: +1-716-645-3733.

E-mail addresses: cjb@buffalo.edu, cjb@eng.buffalo.edu (C. Basaran).

This work studies the electromigration damage in eutectic SnPb flip chip solder joints under current stressing at room temperature with the current density of $1.3 \times 10^4 \text{ A/cm}^2$. Three identical flip chip modules were used in this experiment; all produced in an industrial lab to attain consistent interconnects representative of volume manufacturing. The modules have a silicon test wafer mounted onto an FR-4 printed circuit board (PCB) using eutectic SnPb solder joints. The height of the solder joints was 100 μm . Module #1 was used to perform the electromigration experiment. Modules #2 and #3 were used in nano-indentation tests and provided initial mechanical properties of the solder joint prior to current stressing. Mass accumulation near the anode and void nucleation near the cathode were observed during current stressing. Results from nano-indentation testing on solder joints for electromigration are reported for the first time. Surface marker movement is used to measure the atomic flux driven by electromigration and to calculate the product of effective charge number and diffusivity, $D \times Z^*$, of the solder at room temperature. The effective charge number can be extracted if the solder diffusivity at room temperature is known. Grain coarsening and Pb phase region growth was also observed during the experiment.

2. Electromigration results

Eutectic SnPb solder joints on Module #1 were cross-sectioned and polished for direct observation of electromigration. A schematic cross-section of the solder joint and the scanning electron microscopy (SEM) secondary image of the cross-section are shown in Fig. 1(a) and (b). The specimen was cross-sectioned and polished to the center of the solder joint using 240, 600, and 1200-grit silicon carbide abrasive paper. The joint was subjected to current stressing with 1 A DC at room temperature, yielding an average current density through the solder joint of $1.3 \times 10^4 \text{ A/cm}^2$ based on the diameter of solder joint. The test module was taken off for SEM analysis after 3, 6, 14.5, and 37.5 h of stressing. A nano-indentation experiment was performed on the solder joints of Module #1 after 37.5 h of stressing.

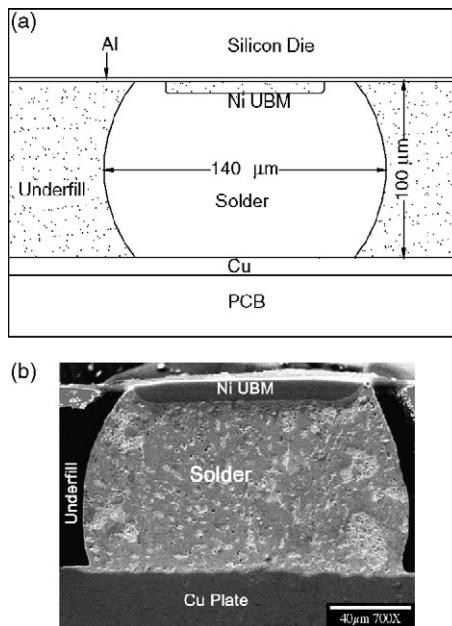


Fig. 1. (a) A schematic cross-section; (b) SEM secondary image (right) of solder joint on Module #3.

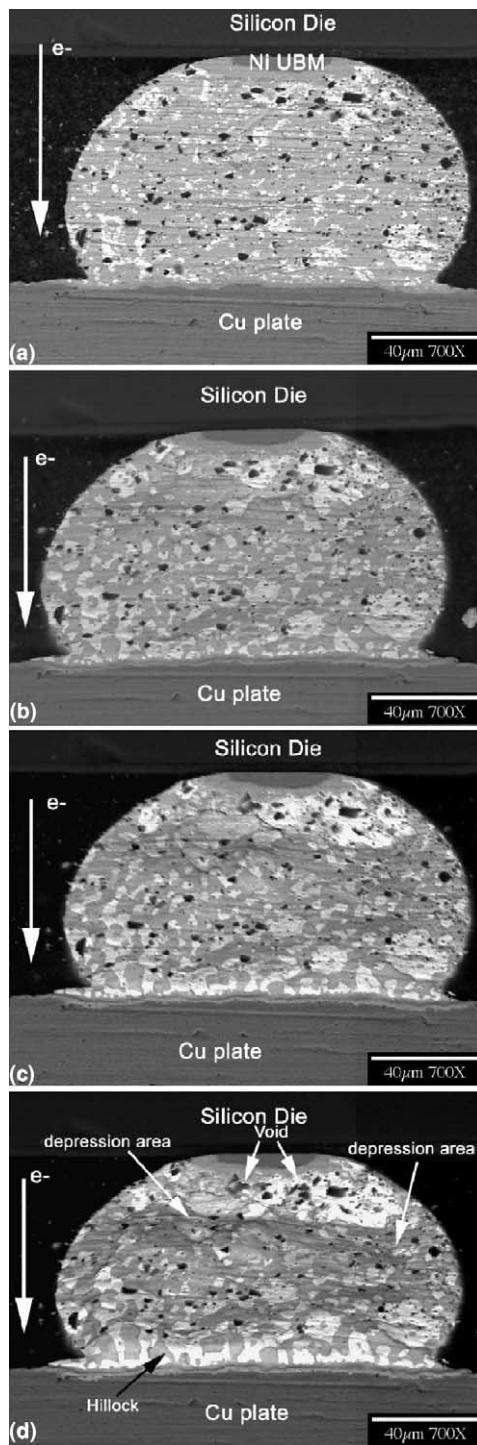


Fig. 2. SEM backscattered image of solder joint on Module #1 for: (a) initial; (b) 6 h; (c) 14.5 h and (d) 37.5 h.

The SEM backscattered images of cross-sectioned surface of solder joint are shown in Fig. 2(a)–(d), for initial, 6, 14.5, and 37.5 h of current stressing, respectively. SEM secondary images of the joint at several magnifications are shown in Fig. 3(a)–(c) for 37.5 h of stressing. The SEM backscattered image gives more information about elemental composition whereas the secondary image gives more topographic information (Goldstern et al., 1992).

The direction of electron flow is from Ni under bump metallization (UBM) on silicon die side to Cu plate on PCB side, or top to bottom in these figures. The mass accumulation on the anode side and the void nucleation on the cathode side can be seen in Figs. 2 and 3. The surface of the cross-sectioned solder joint became very rough after 37.5 h due to electromigration. Large depression areas were formed on the cathode side and big voids formed near the Ni UBM side, indicating large amount of mass depletion in the region.

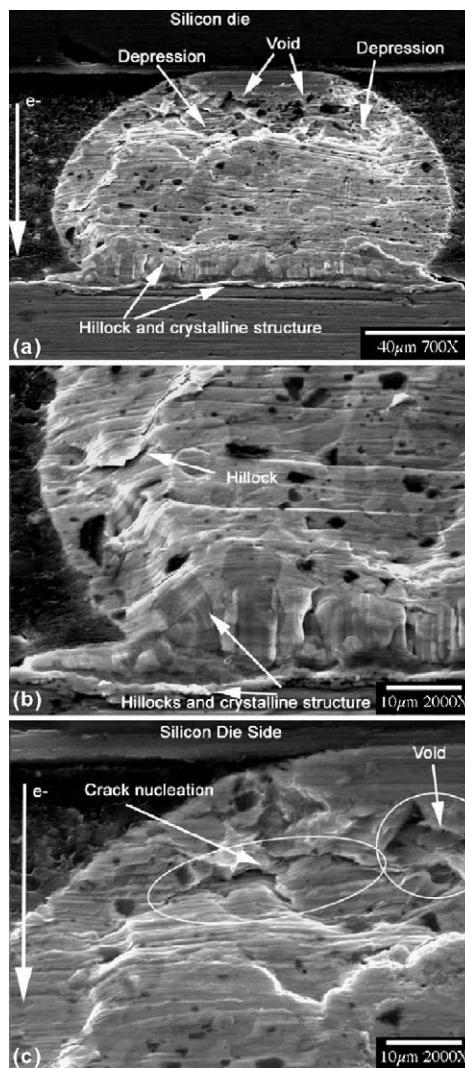


Fig. 3. SEM secondary images for Module #1: (a) after 37.5 h, magnification 700 \times ; (b) area on the PCB board side (anode), 2000 \times ; (c) area on the silicon die side (cathode), 2000 \times .

Hillocks were formed near the Cu plate region due to mass accumulation. Hillocks and crystalline formation were clearly shown in the anode region in Fig. 3(a). Both voids and cracks can be clearly seen in the near cathode region in Fig. 3(c). It is worth to point out that for the solder joint in the real working condition, which is surrounded by epoxy underfill, hillock formation may be impeded. One can expect that much larger compression stress would develop near anode region and tension stress would develop near cathode region compared to the partially exposed cross-sectioned solder joint under test. The development of compressive and tensile stresses will in turn affect the rate of electromigration as in the case of thin film electromigration (Blech and Herring, 1976).

3. Nano-indentation experiment

The ultimate goal of this study is to establish a damage mechanics model for solder joints under current stressing in the frame of thermodynamics by exploring changes in the mechanical properties. Traditional standard mechanical tests are not possible for solder joints because of its small size. A nano-indenter (MTS Nano-indenter XP with Continuous Stiffness Measurement CSM system) with the ability to perform tests on extremely small samples was used to measure the Young's modulus and hardness of solder joints.

Initial mechanical properties of the solder joints before current stressing were obtained from Modules #2 and #3. Then change in mechanical properties due to electrical current stressing was continuously monitored. To perform the nano-indentation testing on solder joints, the test modules need to be cross-sectioned. Diamond wheel saw and 240, 600, and 1200-grit silicon carbide abrasive paper were used to section and polish the sample exposing the mid-section surface of solder joints (half sphere).

Nano-indentation was first performed directly on the cross-sectioned solder joint surface. Six indentations were performed on the solder joints of Module #2. The measured values of Young's modulus and hardness were scattered by more than 50%. For instance, the modulus varied from 40 to 69 GPa and hardness varied from 0.087 to 0.121 GPa. The scattered measurements are reasonable only if they fall into a small range due to the binary alloy nature of solder. But the measurements for this solder joint can only be considered erroneous due to its large variation range.

The nano-indenter precisely measures the indentation force and displacement of the indenter tip in a scale of mN and nm, respectively. Based on these measurements, it computes the position of contact surface and then the indentation depth as well as contact area. The computation of Young's modulus and hardness are based on the measured force, time and computed contact area on the basis of elastic half space theory. If the sample surface is not sufficiently flat and smooth, miscalculation of contact area may occur and lead to inaccuracy of modulus and hardness measurement. SEM imaging verified this, as shown in Figs. 4 and 5.

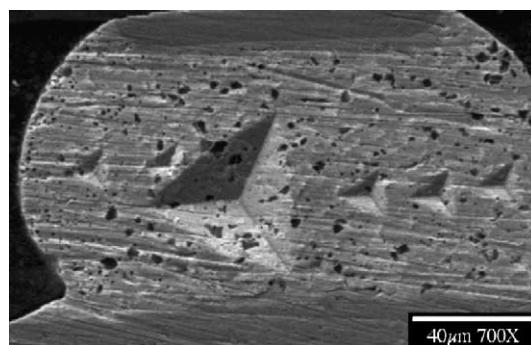


Fig. 4. SEM secondary image of solder joint of Module #2 after nano-indentation test.

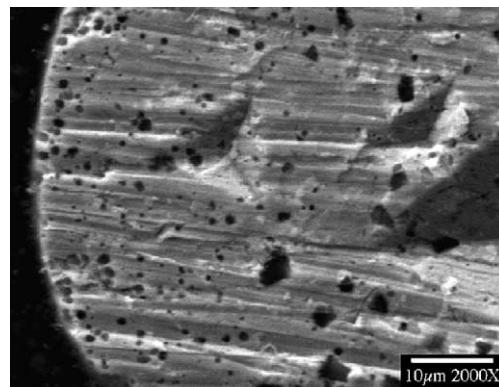


Fig. 5. Large magnification SEM secondary image of solder joint of Module #2 after nano-indentation test.

There were deep scratches on the solder surface compared to the indentation depth (2 μm) due to the polishing with silicon carbide paper. Basaran and Jiang (2002) established the standards for the consistent measurement of elastic modulus of solder joints, using nano-indentation. The same surface preparation procedure was utilized (240, 600, and 1200-grit silicon carbide paper in sequence) by Basaran and Jiang (2002). The sizes of solder joints tested by Basaran and Jiang was 400 μm in height compared to 100 μm flip chip solder joints in this project. The SEM images of 400 μm solder joints, prepared with 1200 grit silicon carbide paper, are much smoother. Although the composition of the solder joints are the same and the same surface preparation procedure is followed, a coarse surface will result for smaller size solder joints. The reason for this is not yet clear. To improve the accuracy of the nano-indentation test and standardize a surface preparation procedure for all the experiments, an ASTM standard was chosen. The ASTM standard E3 (1999b) was applied to the surface preparation for Module #3. First 1200-grit abrasion was used, followed by graded diamond paste and a final polish was 0.05 μm gamma alumina. By following ASTM E3 standard, much better surface finish was achieved on the solder joints of Module #3 as shown in Fig. 1(b). The modulus and hardness measurements on the finely polished solder surface of Module #3 are shown in Table 1. The average modulus is 34.7 GPa with standard deviation of 2.52 (7.3%) and average hardness is 0.21 GPa with deviation of 0.03 (14%).

The Module #1 was taken off the circuit after 37.5 h of 1 A current stressing for nano-indentation tests. First, nano-indentation was performed on the solder joint surface without re-polishing the surface. As shown in Fig. 3(a), the cross-sectioned surface of the solder joint of Module #1 became very rough after 37.5 h of electromigration. Largely scattered measurements on modulus (from 27.3 to 49.9 GPa) and

Table 1
Nano-indentation test on Module #3 (without current stressing)

Module #	3		
	Young's modulus (GPa)	Hardness (GPa)	Indentation depth (nm)
Test 1	35.876	0.231	2000
Test 2	34.721	0.254	2000
Test 3	34.472	0.198	2000
Test 4	30.061	0.155	2000
Test 5	37.436	0.21	2000
Test 6	35.872	0.197	2000
Average	34.7	0.21	

hardness (from 0.141 to 0.336 GPa) were observed as expected as shown in Table 2. Then the solder joint was re-polished following the procedure in ASTM E3 standard. The nano-indentation measurements from the re-polished solder joint of Module #1 are shown in Table 3. The average modulus for the re-polished solder joint of Module #1 is 36.87 GPa and average hardness is 0.2 GPa. After the first set of indentation tests, the residual stress within the solder joint, due to the plastic deformation caused by indentation, may alter its mechanical properties. Indentation depth is only 2 μm , thus plastic deformation only takes place in the region very near to the surface. When the specimen was re-polished, 5 μm thick solder layer was removed from its surface; as a result, the residual stress from the first set of indentation would not affect the results from the second set of indentation.

Elastic modulus and hardness values obtained from Module #1 after current stressing are bigger than the values obtained from Module #3, which was not subjected to electrical current. This observation is contradictory to the expectation that the modulus (or hardness) of a material would decrease as damage nucleates in the material, as always observed in a mechanical or thermal fatigue experiments. The reason for this observation is that although the composition of the solder joints and manufacturing processes in these two modules are assumed to be the same; there are initial mechanical property differences. This was verified by performing indentation tests on more than 50 flip chip solder joints without current stressing, all following ASTM E3 surface preparation procedure. The measured Young's modulus for these solder joints ranged from 27 GPa to 50 MPa, with a 95% confidence level for the interval of 39.4 GPa to 41.7 MPa.

Based on this finding, the authors proposed an improved experiment scheme, which will be used in the future experiments. In this new scheme, nano-indentation test will be performed on a solder joint before it is subjected to current stressing to get the initial mechanical properties of this particular solder. Then this solder joint will be re-polished and subjected to electromigration. After current stressing, the solder will be re-polished again and be applied to nano-indentation test to get the change of mechanical properties after

Table 2
Nano-indentation test on Module #1 after 37.5 h of current stressing (without re-polishing)

Module #	1		
	Young's modulus (GPa)	Hardness (GPa)	Indentation depth (nm)
Test 1	39.772	0.246	2000
Test 2	27.322	0.141	2000
Test 3	49.916	0.336	2000
Test 4	38.905	0.269	2000
Test 5	46.459	0.322	2000
Average	40.47	0.26	

Table 3
Nano-indentation test on Module #1 after 37.5 h of current stressing (re-polished following procedure in ASTM E3 standard)

Module #	1		
	Young's modulus (GPa)	Hardness (GPa)	Indentation depth (nm)
Test 1	34.733	0.214	2000
Test 2	35.55	0.178	2000
Test 3	41.405	0.229	2000
Test 4	37.613	0.183	2000
Test 5	34.844	0.184	2000
Test 6	36.961	0.257	2000
Test 7	36.986	0.182	2000
Average	36.87	0.20	

electromigration. This scheme is possible since the indentation depth can be controlled to 2 μm and thus only a very thin layer (several microns) needs to be polished away after indentation.

4. Analysis of electromigration through marker displacement

In order to measure the atomic flux in the solder joint due to current stressing, inert particles on the sectioned solder surface were used as markers. The markers were SiC particles left on the surface during polishing. The Cu plate/solder interface was chosen as the fixed frame of reference. This method was reported by Lee et al. in their electromigration experiment (Lee et al., 2001).

The markers position and their movement are shown in Figs. 6 and 7. All the markers have moved to the cathode side, which is the opposite direction of the electromigration flux. The measurement of marker movement was done by measuring the change in marker position with respect to the reference frame on the SEM backscatter images after 6, 14.5 and 37.5 h of current stressing. The average movement of the markers, as the dashed line in Fig. 8, shows a near linear dependence on current stressing time. This observation is in consistence with Lee and Tu's observation (Lee and Tu, 2001).

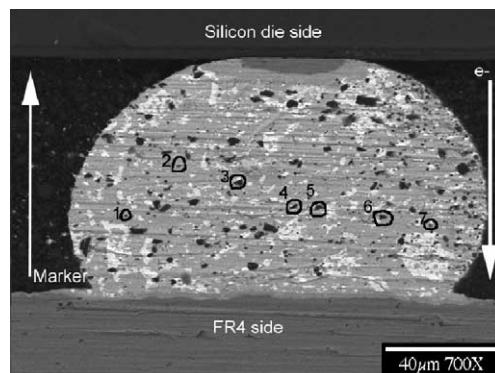


Fig. 6. Markers position on the cross-sectioned surface (initial SEM backscatter image).

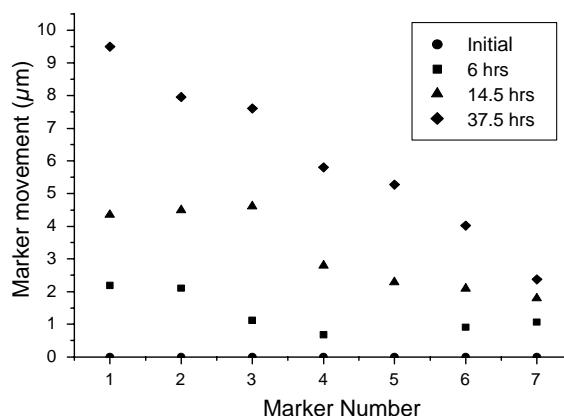


Fig. 7. The marker movement on the sectioned eutectic SnPb surface.

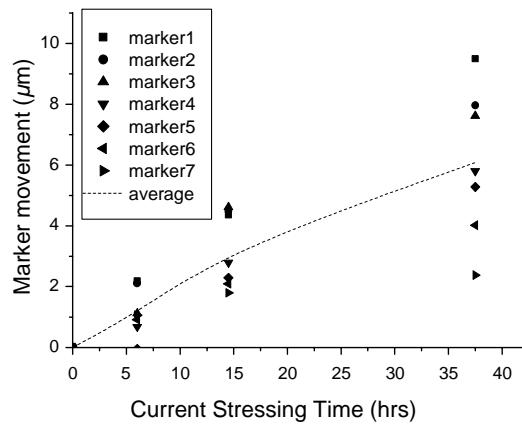


Fig. 8. The marker movement vs. current stressing time.

5. Calculation of $D \times Z^*$ in solder joint

The atomic flux due to electromigration can be calculated from the marker movement, stressing time, and cross-sectional area of solder at the initial marker position (Tu, 1992),

$$J_{\text{atom}} = \frac{V_{\text{EM}}}{\Omega \cdot A \cdot t} = C \frac{D}{kT} Z^* \cdot e \cdot \xi \quad (1)$$

where

V_{EM}	the volume of solder moved by electromigration, cm^3
Ω	the average atomic volume of the solder, cm^3/atom
A	the cross-sectional area at the initial marker position, cm^3
t	the time of current stressing, s
C	the number of atoms per unit volume, atoms/cm^3 (assumed to be $1/\Omega$ in a unary system)
D	the diffusivity, cm^2/s
k	8.617×10^{-5} eV/K (the Boltzmann's constant)
T	the temperature in K
Z^*	the effective charge number
e	the electron charge
ξ	the electrical field, V/cm

The volume of solder moved by electromigration, V_{EM} , is calculated from the average marker movement (Lee et al., 2001). In this experiment, the V_{EM} is calculated to be $4.51 \times 10^{-8} \text{ cm}^3$ after 37.5 h of current stressing. The cross-sectional area of solder joint at the initial marker position is $7.697 \times 10^{-5} \text{ cm}^2$. The average marker movement is 6.078 μm . The electrical field is calculated with a eutectic SnPb solder resistivity of $15 \mu\Omega\text{cm}$ at room temperature and the current density is calculated from the measured current and the cross-sectional area of solder joint at the initial marker position. In this experiment, the stressing current is 1 A so that the current density is $1.3 \times 10^4 \text{ A/cm}^2$ and the electrical field $\xi = \rho j = 15 \times 10^{-6} \times 1.3 \times 10^4 = 0.195 \text{ V/cm}$.

The value of $D \times Z^*$ is thus computed and compared to Lee et al.'s and Lee and Tu's test results (Lee and Tu, 2001) as shown in Table 4. The difference between Lee et al.'s as well as Lee and Tu's experiments and present one is that their experiment was performed at elevated temperature 120 °C and present experiment

Table 4
Comparison of $D \times Z^*$

	Lee et al. (2001)	Lee and Tu (2001)	Present
Temperature (°C)	120 °C	120 °C	Room temperature
Current density (A/cm ²)	2×10^4	3.8×10^4	1.3×10^4
Time (h)	324	39.5	37.5
$D \times Z^*$	2.16×10^{-11}	1.85×10^{-10}	5.62×10^{-10}

was done at the room temperature. Comparison of these test results is shown in Table 4. With $D \times Z^*$ measured and the diffusivity of solder at room temperature known, the effective charge number Z^* can be extracted.

6. Grain coarsening and Pb-phase region growth

Coarsening in PbSn eutectic solder joints is very often used as a degradation metric. When the average phase size exceeds a pre-set critical size the solder joint is assumed to be a failed joint. Electrical current induced coarsening should be no different. Grain coarsening and phase growth (Callister, 1996) of eutectic solder alloys due to thermal cycling or strain has been extensively reported in the literature. Grain coarsening is covered by several models for bulk metals and verified for flip-chip solder joints by Wen and Basaran (2003). Since electromigration is a diffusion process driven by a high-density direct current or electron wind, phase growth is expected. Mass accumulation in the anode side, void formation in cathode side and coarsening of a Pb-phase region were observed during experimentation.

The Pb phase growth of joints was measured along the current stressing course following ASTM standard E1382 (1999a). According to ASTM standard E1382, several methods can be used to determine average grain size: grain intercept lengths, intercept counts, intersection counts, grain boundary length, and grain areas. Individual grain area method for two-phase structure is used in this experiment by means of a digital imaging processing software. The area of each Pb phase interior, A_i , on the solder surface is measured for every Pb phase region. The average phase region area, \bar{A}_{Pb} , is determined by

$$\bar{A}_{\text{Pb}} = \frac{\sum_{i=1}^N A_i}{N_{\text{Pb}}} \quad (2)$$

where N_{Pb} is the total number of Pb phase regions on the solder surface.

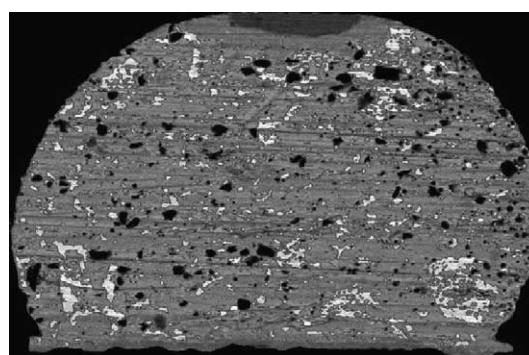


Fig. 9. Pb phase region outlined by Image Pro Plus®.

The average Pb phase region area was measured for solder joints before current stressing, after 3, 6, 14.5, and 37.5 h of stressing at 1.3×10^4 A/cm². The average phase area was measured directly on the SEM backscattered images of cross-sectioned solder joint. Due to extensive mass accumulation and void nucleation under electromigration after 37.5 h of current stressing, the solder joint needed re-polishing prior to measurement.

Media Cybernetics' image analysis software Image Pro Plus[®] (2000) was used to automatically identify the phase region boundary, and measure phase area and average diameter. On SEM backscatter image, the light region corresponds to the Pb rich region and dark region corresponds to the Sn rich region because of their difference in element numbers in the periodic table. By setting the gray scale limits in Image Pro Plus[®], the Pb rich region boundary can be detected, and area, diameter and size data measured. The Pb phase region is outlined as shown in Fig. 9.

The average area and diameter of Pb rich regions grew with increased current stressing as shown in Table 5. The "average diameter" is derived from the average length of several lines drawn through the centroid of the phase region and only the "average area" is an ASTM standard (E1382).

Conversely, the count of Pb rich regions decreased during increased current stressing indicating that the Pb diffused to the anode to form large regions while small Pb phase regions disappeared. SEM image and EDX analysis confirmed this. It can be concluded that Pb is the primary diffusion species in the electromigration of eutectic PbSn solder at room temperature. This observation is different from the observation of Liu and others (Liu et al., 1999), where Sn was found to be the dominant diffusion species in their room temperature electromigration test. Curves of average Pb phase size and average Pb phase diameter of Pb regions vs. stressing time are shown in Fig. 10.

Table 5
Average Pb phase area, diameter and counts

	Area (μm ²)	Diameter (μm)	Phase counts
0 h	4.045516	1.752161	541
3 h	9.581432	2.397059	368
6 h	12.15295	2.664739	334
14.5 h	17.34397	2.999451	216
37.5 h	22.68222	3.38025	163

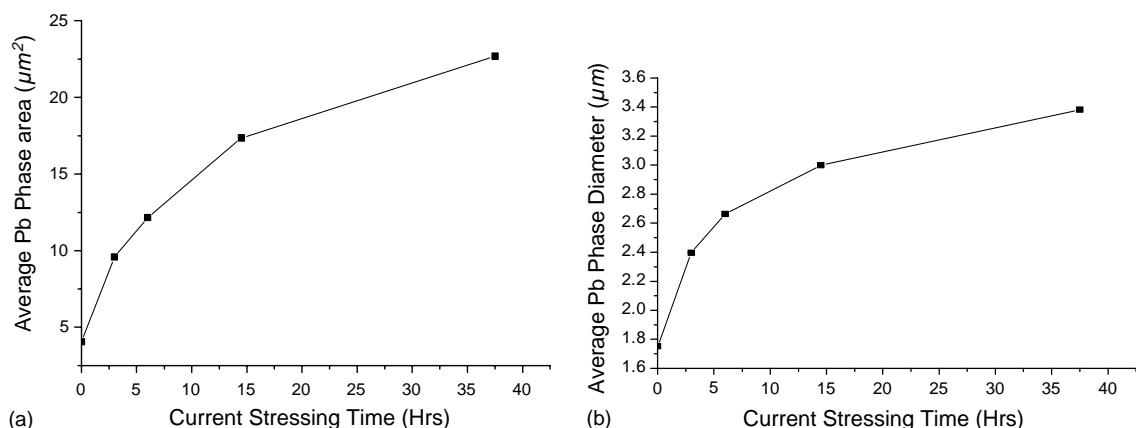


Fig. 10. Pb phase: (a) average area vs. stressing time; (b) average diameter vs. stressing time.

7. Conclusions

The main goal of this project is to identify the mechanism of electromigration damage in microelectronics solder joints. Eutectic SnPb 100 μm in height solder joints were studied under electrical current stressing at room temperature with the current density of $1.3 \times 10^4 \text{ A/cm}^2$. Mass accumulation near the anode and void nucleation near the cathode were observed during current stressing. Nano-indentation was used to observe mechanical property degradation on solder joints under high current density. Surface marker movement was used to measure the atomic flux driven by electromigration and to calculate the product of effective charge number and diffusivity, $D \times Z^*$, at room temperature. The effective charge number can be extracted if the solder diffusivity at room temperature is known. Grain coarsening and Pb phase growth during electromigration was observed with SEM.

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